Vertex Standard

# VX-1700 Series

## HF Multi Mode Mobile Radio Service Manual

***For USA Version***

 EC051H95A

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## *Introduction*

This manual provides the technical information necessary for servicing the VX-1700 HF Transceiver.

Servicing this equipment requires expertise in handing surface-mount chip components. Attempts by non-qualified persons to service this equipment may result in permanent damage not covered by the warranty, and may be illegal in some countries.

Two PCB layout diagrams are provided for each double-sided board in this transceiver. Each side of the board is referred to by the type of the majority of components installed on that side ("Side A" or "Side B"). In most cases one side has only chip components (surface-mount devices), and the other has either a mixture of both chip and leaded components (trimmers, coils, electrolytic capacitors, ICs, etc.), or leaded components only.

As described in the pages to follow, the advanced microprocessor design of the VX-1700 Transceiver allows a complete alignment of this transceiver to be performed without opening the case of the radio; all adjustments can be performed from the front panel, using the "Alignment Mode" menu.

While we believe the information in this manual to be correct, VERTEX STANDARD assumes no liability for damage that may occur as a result of typographical or other errors that may be present. Your cooperation in pointing out any inconsistencies in the technical information would be appreciated.

## Contents

# *Specifications*

## *General*

**Receiver Frequency Range**: 30 kHz ~ 30.0000 MHz
**Transmitter Frequency**: 1.600 ~ 30.0000 MHz
**Emission Modes**: A1A (CW), J3E (LSB/USB), A3E (AM), J2B (USB/LSB),
**Frequency Synthesizer Step**: 10 Hz, 100 Hz, 1 kHz
**Frequency Stability**: ±1 ppm (Typical)
**Operating Temperature Range**: 14° F ~ 131° F (–10° ~ +55° C) @Duty Cycle TX:RX = 1 min.: 4 min.
**Antenna Impedance**: 50 Ohms
**Supply Voltage**: 13.8 Volts DC ±15%, negative ground
**Power Consumption**: 25 mA (Standby)
1.0 A (Receive, no signal)
1.5 A (Receive)
22 A (Transmit, 125 Watts output)
**Dimensions** (WxHxD): 9.5″ x 3.9″ x 11.2″ (241 x 99 x 285 mm)
**Weight** (approx.): 9.5 lbs (4.3 kg)

## *Transmitter*

**Power Output**: 125 Watts (A1A, J2B, J3E @1.6000 ~ 3.9999 MHz)
100 Watts (A1A, J2B, J3E @4.0000 ~ 30.0000 MHz)
31 Watts AM Carrier (A3E @1.6000 ~ 3.9999 MHz)
25 Watts AM Carrier (A3E @4.0000 ~ 30.0000 MHz)
**Modulation Types**: J3E: PSN type modulator,
A3E: Low-level (early stage)
**Spurious Radiation**: Better than –56 dB
**J3E Carrier Suppression**: Better than 50 dB below peak output
**Undesired Sideband Suppression**: Better than 60 dB below peak output
**J3E Audio Response**: Not more than –6 dB from 400 Hz ~ 2500 Hz
**Occupied Bandwidth**: A1A: less than 0.5 kHz
J3E: less than 3.0 kHz
A3E: less than 6.0 kHz
**Microphone Impedance**: 200 ~ 10 k Ohms (600 Ohms Nominal)

## *Receiver*

**Circuit Type**: Double-conversion Superheterodyne
**Intermediate Frequencies**: 1st: 45.274 MHz, 2nd: 24 kHz
**Sensitivity**:

| | A1A/J2B/J3E | A3E |
|---|---|---|
| 0.1 ~ 0.5 MHz | — | — |
| 0.5 ~ 1.6 MHz: | 1.41 μV | 8 μV |
| 1.6 ~ 30 MHz: | 0.16 μV | 1 μV |

(A1A/J2B/J3E/A3E: S/N 10 dB)

**Squelch Sensitivity** (A1A/J2B/J3E):

| | |
|---|---|
| 0.1 ~ 0.5 MHz | — |
| 0.5 ~ 1.6 MHz: | 2.5 μV |
| 1.6 ~ 30 MHz: | 2 μV |

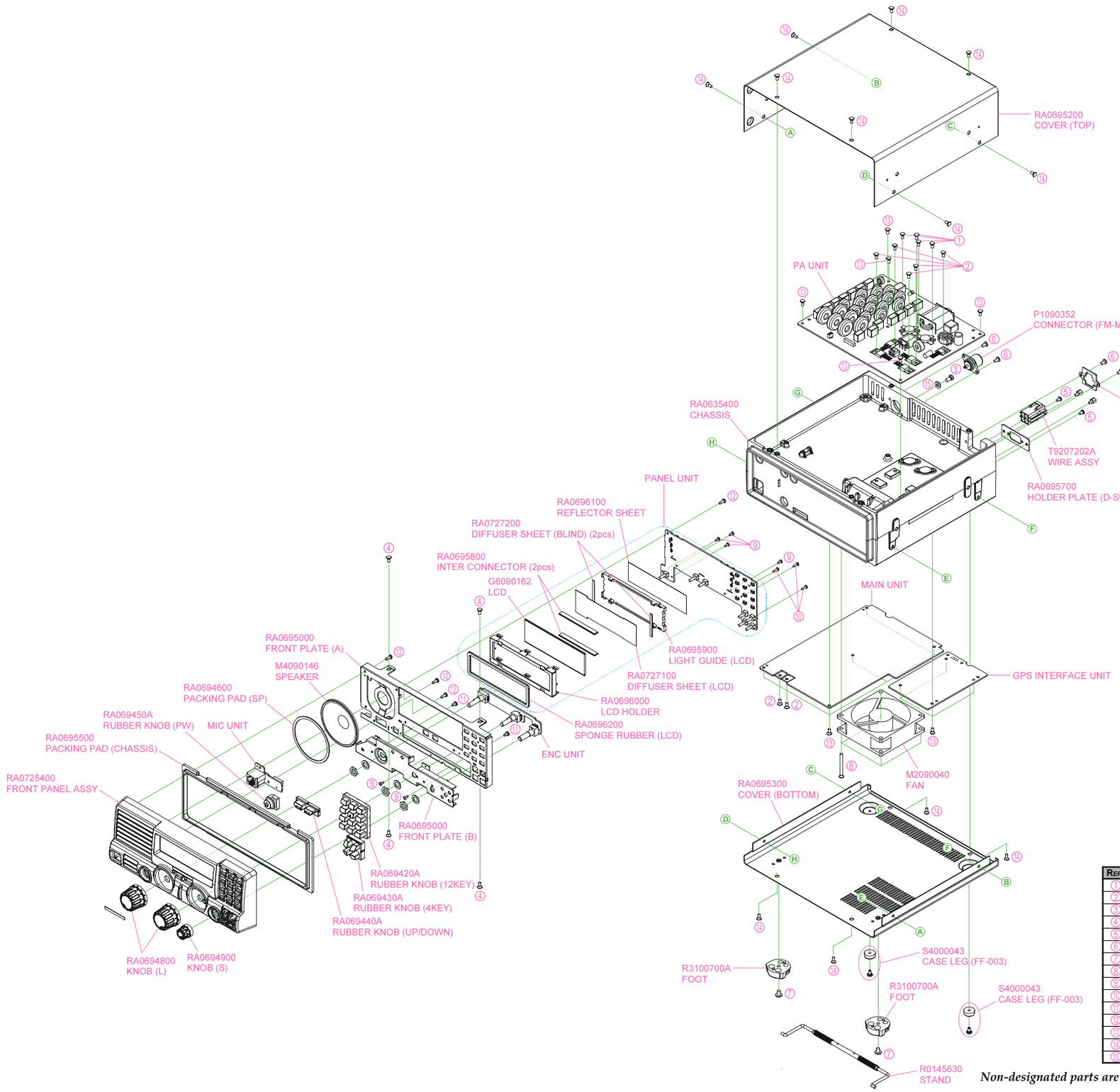
**IF Rejection**: Better than 80 dB
**Image Rejection**: Better than 80 dB
**Selectivity**:

| | –6 dB | –60 dB |
|---|---|---|
| A1A(W), J2B(W), J3E | > 2.2 kHz | < 4.5 kHz |
| A1A(N), J2B(N) | > 500 Hz | < 2.0 kHz |
| A3E | > 6 kHz | < 20 kHz |

**Audio Output**: At least 2.2 Watts into 8 Ohms @ 10% THD
**Audio Output Impedance**: 4 ~ 16 Ohms (8 Ohms Nominal)
**Conducted Radiation**: Less than 4000 μμW

*Specifications are subject to change without notice or obligation.*

# *Exploded View & Miscellaneous Parts*




| Supplied Accessories | | |
|---|---|---|
| VXSTD P/N | Description | Qty. |
| A06870001 | MH-31A8J Hand Microphone | 1 |
| T9023725 | DC Power Cord | 1 |
| Q0000074 | Spare Fuse (25 A Blade Type) | 1 |

| Connection Cables | | |
|---|---|---|
| Ref. | VXSTD P/N | Description |
| P0001 | T9315504 | Coaxial Cable (J1001↔J2006) |
| P0002 | T9315905 | Coaxial Cable (J1002↔J2001) |
| P0004 | T9207203 | 30-pin Flat Cable (J1003↔J2002) |
| P0005 | T9207210 | 13-pin Molex (J1008↔J4001) |
| P0006 | T9207211 | 8-pin Molex (J1005↔J6002) |
| P0007 | T9207209 | 8-pin Molex (J3004↔J6101) |
| P0008 | T9207117A | 30-pin Flat Cable (J1004↔J3001) |

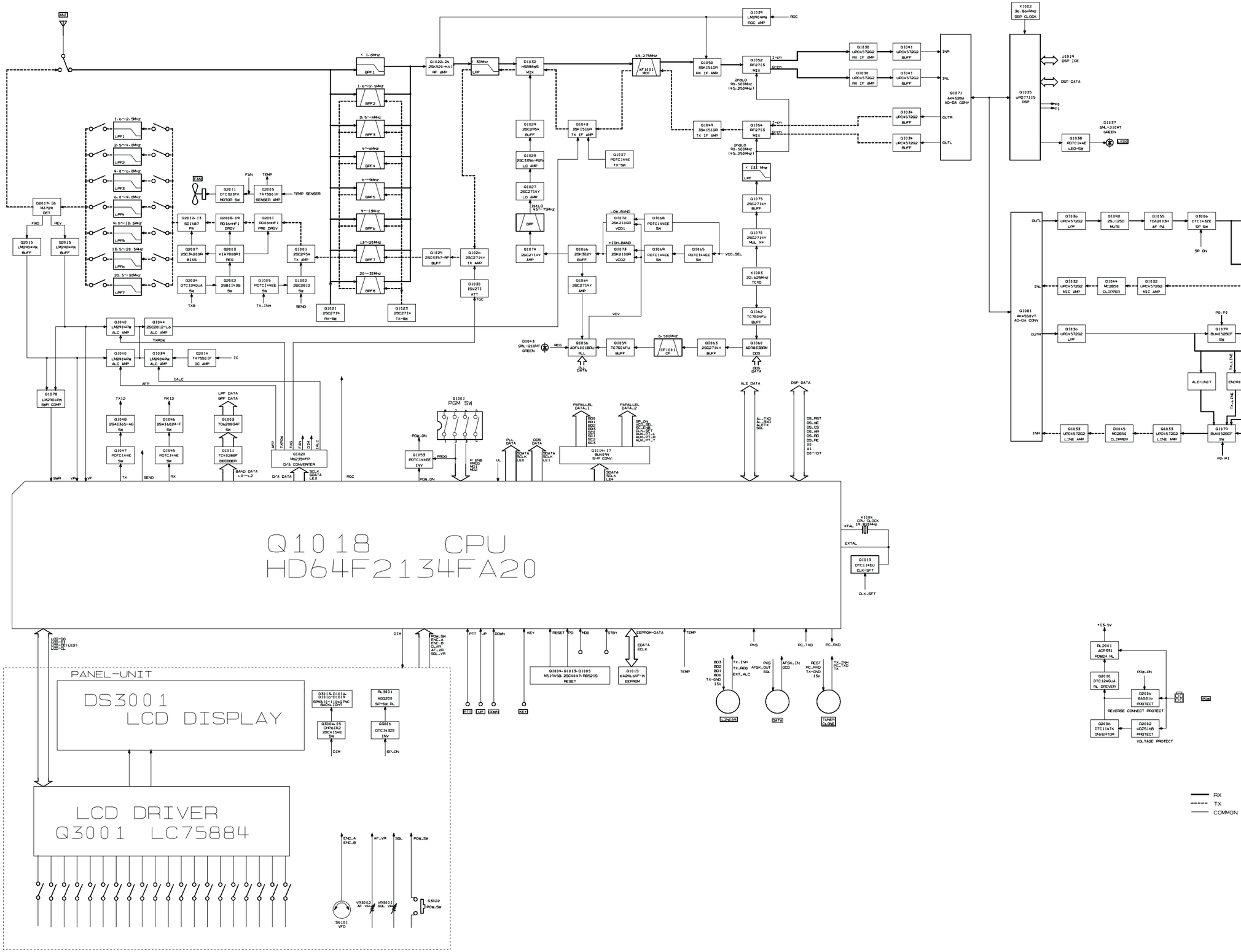
| Ref. | VXSTD P/N | Description | | Qty. |
|---|---|---|---|---|
| ① | U02308002 | SEMS SCREW | SM3X8NI | 4 |
| ② | U03308002 | SEMS SCREW | ASM3X8NI | 7 |
| ③ | U04410002 | SEMS SCREW | HSM4X10NI | 1 |
| ④ | U10306001 | TRUSS HEAD SCREW | M3X6 | 4 |
| ⑤ | U20205002 | BINDING HEAD SCREW | M2.6X5NI | 2 |
| ⑥ | U20306002 | BINDING HEAD SCREW | M3X6NI | 4 |
| ⑦ | U20406007 | BINDING HEAD SCREW | M4X6B | 2 |
| ⑧ | U20430002 | BINDING HEAD SCREW | M4X30(Ni) | 4 |
| ⑨ | U24106002 | TAPTITE SCREW | M2X6NI | 6 |
| ⑩ | U24108002 | TAPTITE SCREW | M2X8NI | 3 |
| ⑪ | U24206001 | TAPTITE SCREW | M2.6X6 | 2 |
| ⑫ | U24208002 | TAPTITE SCREW | M2.6X8NI | 4 |
| ⑬ | U24308002 | TAPTITE SCREW | M3X8NI | 14 |
| ⑭ | U31306007 | OVAL HEAD SCREW | M3X6B | 12 |
| ⑮ | U70004012 | PLAIN WASHER | FW4BSNI | 1 |

*Non-designated parts are available only as part of a designated assembly.*

## *Exploded View & Miscellaneous Parts*

***Note***

# Block Diagram

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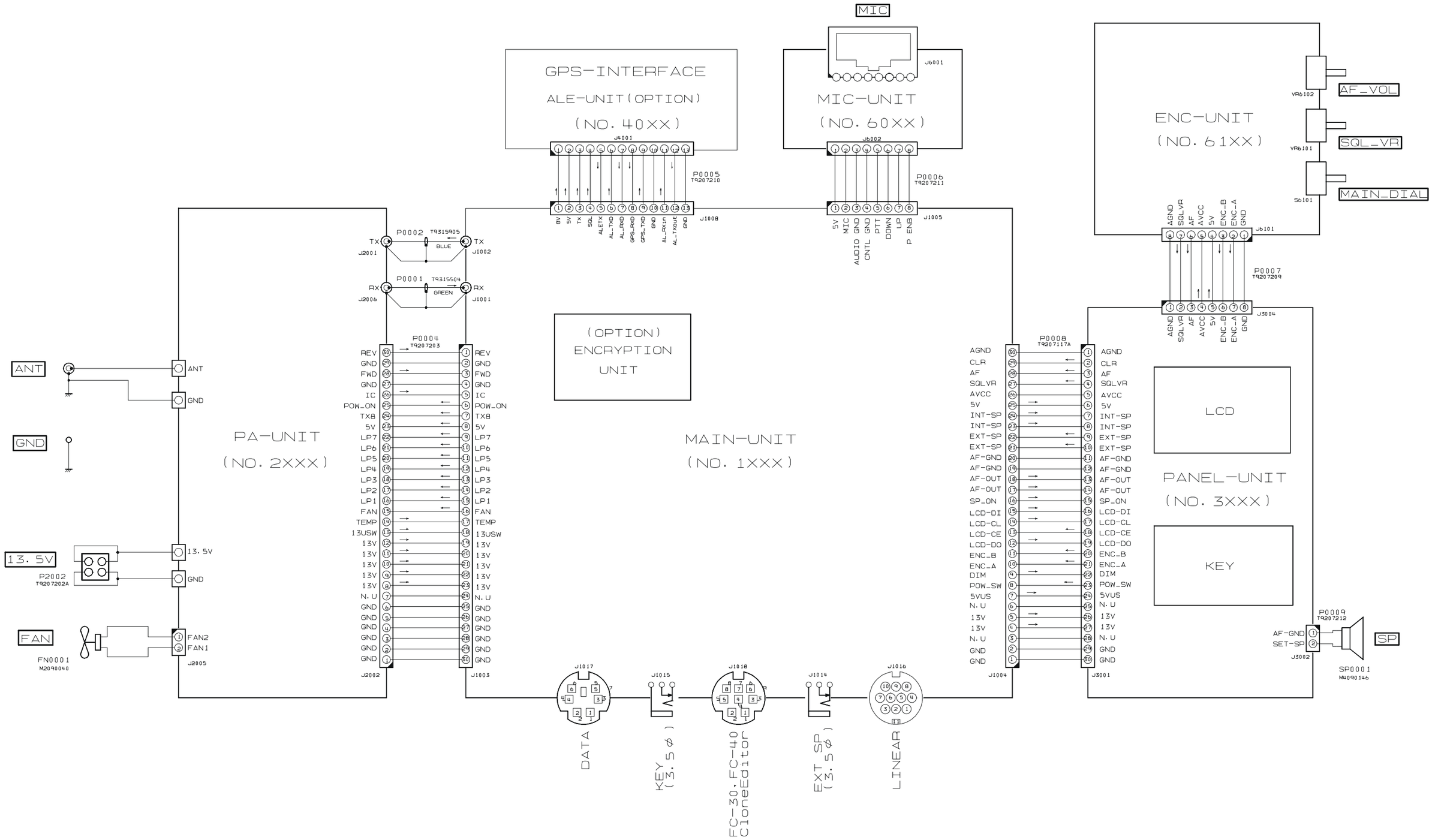
# *Connection Diagram*



## Receive Signal Path

Incoming RF signal from the ANT jack is delivered to the PA Unit, and passes through the TX/RX relay RL2009 to J2006.

The RF signal is then applied to J1001 on the MAIN Unit, and passed through the limiter circuit consisting of **D1006**, **D1007**, **D1008**, and **D1009** (all **RLS245**) to prevent distortion from high RF signal input, and is fed to one of eight band-pass filters which strip away unwanted signals prior to delivery of the incoming signal to the RF amplifiers, **Q1022** and **Q1024** (both **2SK520-K41**).

The amplified RF signal passes through a low-pass filter to the doubly-balanced mixer **D1032** (**HSB88WS**), where the RF signal is mixed with the 1st local signal delivered from buffer amplifier **Q1029** (**2SC2954**), resulting in a 45.274 MHz 1st IF signal.

The 45.274 MHz 1st IF signal is fed through monolithic crystal filter **XF1001**, which strips away unwanted mixer products, and is amplified by 1st IF amplifier **Q1050** (**3SK151GR**); the 1st IF signal is then applied to the 2nd mixer **Q1052** (**RF2713**), where it is mixed with the 45.25 MHz 2nd local signal which is divided from 90.5 MHz reference signal delivered from buffer amplifier **Q1075** (**2SC2714Y**), resulting in a 24 kHz 2nd IF signal.

The 24 kHz 2nd IF signal is fed through buffer amplifiers **Q1030** and **Q1041** (both **UPC4572G2**) to the A/D converter **Q1071** (**AK4528A**), then delivered to the DSP IC **Q1035** (**UPD77115**), where the 24 kHz 2nd IF signal is demodulated in accordance with the mode selection data from the main CPU **Q1018** (**HD64F2134**). The demodulated signal is delivered to the D/A converter **Q1081** (**AK4550VT**) which converts the demodulated signal to audio.

The audio signal from the D/A converter **Q1081** (**AK4550VT**) is fed through a low-pass filter at **Q1036** (**UPC4572G**), which eliminates high-pitched noise on the audio signal, and is fed to the AF mute gate **Q1092** (**2SJ125D**), then applied to the audio amplifier **Q1055** (**TDA2003H**). The amplified audio signal is delivered to J3001 on the PANEL Unit, then passes through the speaker switch RL3001/**Q3006** (**DTC143ZE**) to the internal or external speaker.

The DSP IC **Q1035** (**UPD77115**) outputs AGC data which is proportionate to the received signal strength to the main CPU **Q1018** (**HD64F2134**). The main CPU **Q1018** (**HD64F2134**), in turn, outputs a DC voltage in accordance with the received signal strength. This DC voltage is fed through buffer amplifier **Q1039** (**LM2904PW**) to RF amplifiers **Q1022** & **Q1024** (both **2SK520**) and gate 2 of IF amplifier **Q1050** (**3SK151GR**), to reduce their gains when strong signals are present in the receiver passband.

## Transmit Signal Path

The speech audio from the microphone is delivered to J6001 on the MIC Unit, then applied to J1005 on the MAIN Unit.

The speech audio is amplified by **Q1032-1** (**UPC4572G2**), then passed though the clipper, **D1044** (**MC2850**), and further amplified by **Q1032-2** (**UPC4572G2**).

The amplified speech audio is fed through the A/D converter **Q1081** (**AK4550VT**), then delivered to the DSP IC **Q1035** (**UPD77115**), where the speech audio is modulated in the 24 kHz TX 1st IF signal in accordance with the mode selection data from the main CPU, **Q1018** (**HD64F2134**).

The modulated signal is fed through the D/A converter **Q1071** (**AK4528A**) and buffer amplifier **Q1034** (**UPC4572G2**) to the mixer **Q1054** (**RF2713**) where the 24 kHz TX 1st IF signal is mixed with 1st local signal delivered from buffer amplifier **Q1075** (**2SC2714Y**), resulting in a 45.274 MHz IF signal.

The resulting 45.274 MHz IF signal is buffered by **Q1049** (**3SK151GR**), then delivered to the monolithic crystal filter **XF1001**, which strips away unwanted mixer products, and then is amplified by **Q1043** (**3SK151GR**). The amplified IF signal is delivered to doubly-balanced mixer **D1032** (**HSB88WS**), where it is mixed with the PLL local signal from the buffer amplifier, **Q1029** (**2SC2954**).

The resulting the RF signal at the transmit frequency is fed through a low-pass filter circuit, and then is amplified by **Q1026** (**2SC2714Y**) and buffer amplifier **Q1025** (**2SC3357**), and then filtered by one of eight band-pass filters to suppress out-of-band responses. The RF signal is then amplified by **Q1001** (**2SC2954**) and delivered to the PA Unit.

# Circuit Description

On the PA Unit, the low-level RF signal from the MAIN Unit is amplified by pre-driver **Q2001** (**RD06HHF1**), push-pull driver **Q2008**/**Q2009** (both **RD16HHF1**), and push-pull final amplifier **Q2012**/**Q2013** (both **SD1405**), which provides up to 120 watts of RF output power.

The RF output from the final amplifier is fed through the one of seven low-pass filters, sampling directional coupler T2005, and TX/RX relay RL2009 before delivery to the antenna jack.

The sampling directional coupler senses forward and reverse power output, which is rectified by **D2017** and **D2018** (both **MA729**), respectively, and the DC voltage is then amplified by **Q2015** (**LM2904PW**) on the PA Unit.

The DC voltages derived from forward and reverse power are applied to J1003 on the MAIN Unit, and then amplified by **Q1040** (**LM2904PW**) and **Q1044** (**2SC2812**). The amplified DC voltage is fed back to the 2nd gate of the 45.275 MHz IF amplifier **Q1043** (**3SK151GR**), so that the transmitter's IF gain can be regulated by this sensing of the power output, preventing overdrive or damage caused by transmission into an excessive impedance mismatch at the antenna.

## PLL Circuit

The PLL local signal for the receiver 1st local and the transmitter final local is generated by one of two VCOs: **Q1072** or **Q1073** (both **2SK210GR**) in conjunction with varactor diodes **D1047**, **D1048**, **D1049**, **D1050**, **D1051**, **D1052**, **D1053**, and **D1054** (all **HVU359**) on the MAIN Unit. The oscillating frequency is determined primarily by the level of DC voltage applied to the varactor diodes. The VCO output is buffered by **Q1066** (**2SK302Y**), amplified by **Q1074** (**2SC2714Y**), and band-pass filtered by capacitors C1389, C1391, C1397, C1400, C1409, and C1420 and coils L1070, L1071, L1074, and L1076. The filtered PLL local signal is fed through buffer amplifiers **Q1027** (**2SC2714Y**), **Q1028** (**2SC3356**), and **Q1029** (**2SC2954**) to the TX final mixer or RX 1st mixer **D1032** (**HSB88WS**).

A portion of the output of buffer amplifier **Q1066** (**2SK302Y**) is further amplified by **Q1064** (**2SC2714Y**), then delivered to the PLL subsystem IC **Q1056** (**ADF4001BRU**), which contains a reference divider, serial-to-parallel data latch, programmable divider, phase comparator and a swallow counter. The sample VCO signal is divided by the programmable divider section of the **Q1056** (**ADF4001BRU**). Meanwhile, the output from the 22.625 MHz TCXO reference oscillator, **X1003**, is amplified by **Q1062** (**TC7S04FU**) and divided by the DDS IC **Q1060** (**AD9833BRM**) in accordance with the PLL dividing data from the main CPU, **Q1018** (**HD64F2134**), then fed through the buffer amplifiers **Q1063** (**2SC2714Y**) to ceramic filter **CF1001**. The divided and filtered reference signal is applied to the reference divider section of the PLL subsystem IC **Q1056** (**ADF4001BRU**), where it is divided by 25/26 to produce the loop reference.

The divided signal from the programmable divider (derived from the VCO), and that derived from the reference oscillator, are applied to the phase detector section of the PLL subsystem IC **Q1056** (**ADF4001BRU**), which produces a pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is fed through the loop filter, consisting of resistors R1222, R1233, & R1247 and capacitors C1278, C1284, C1298, C1308, & C1418, then fed back to the VCO varactor diodes **D1047**, **D1048**, **D1049**, **D1050**, **D1051**, **D1052**, **D1053**, and **D1054** (all **HVU359**).

Changes in the DC voltage applied to these varactor diodes affect the reactance in the tank circuit of VCOs **Q1072** and **Q1073** (both **2SK210GR**), changing the oscillating frequency according to the phase difference between the signals derived from the VCO and the TCXO reference oscillator. The VCO is thus phase-locked to the reference frequency standard.

A portion of the output of reference signal from TCXO **X1003** is multiplied by four at **Q1070** (**2SC2714Y**). The resulting 90.5 MHz signal is buffered by **Q1075** (**2SC2714Y**), then applied to a low-pass filter, consisting of capacitors C1401, C1405, C1410, C1411, and C1421 and coils L1075 and L1077. The filtered reference signal is applied to the TX 1st mixer **Q1054** and RX 2nd mixer **Q1052** (both **RF2713**).

## Control Circuit

Major frequency control functions such as channel selection, display, and PLL divider control are performed by main CPU **Q1018** (**HD64F2134**) on the MAIN Unit, at the command of the user via the tuning knob and function switches on the front panel.

The programmable divider data for the PLL from the main CPU is applied directly to DDS IC **Q1016** (**AD9833BRM**) and PLL subsystem IC **Q1056** (**ADF4001BRU**).

The Mode selection data from the main CPU is also delivered to DSP IC **Q1035** (**UPD77115**) to control the various circuits required for the selected mode.

The Band selection binary data from the main CPU is decoded (BCD to Decimal) by **Q1011** (**TC4028BF**). The resulting decimal outputs are level-shifted by **Q1003** (**TD62783AF**) to select the active band-pass filter on the MAIN Unit required for the operating frequency. Also, the decimal outputs from **Q1003** (**TD62783AF**) are delivered to PA Unit, where they are used to select the active low-pass filter required for the operating frequency.

## TX/RX Control

When the PTT switch is pressed, pin 21 of the main CPU **Q1018** (**HD64F2134**) goes low, which causes pin 60 of the main CPU **Q1018** (**HD64F2134**) to go low. This signal disables the receiver 12 V bus at **Q1046** (**2SA1602A**). At the same time, pin 59 of the main CPU **Q1018** (**HD64F2134**) goes low to activate the transmit 12 V bus at **Q1048** (**2SA1365**).

## Power Supply & Regulation

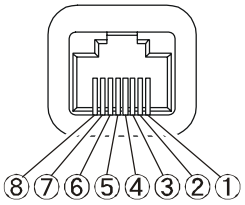
The +5 V bus for the main CPU **Q1018** (**HD64F2134**) is derived from the 13.5 V bus via regulator **Q1012** (**BA05FP**) on the MAIN Unit. The +8 V bus is derived from the 13.5 V bus via regulator **Q1007** (**KIA7808API**) on the MAIN Unit.

A portion of the +8 V bus is regulated by **Q1008** (**L78M05T**) for the +5 V bus, and is regulated by **Q1006** (**UPC2926**) for the +2.6 V bus required by the DSP IC **Q1035** (**UPD77115GK**).

# *Connector Pinout Diagrams*

## MIC Jack

**(As Viewed From Front Panel)**

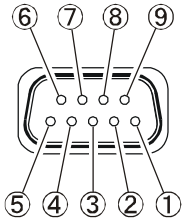



① P ENB
② CNTL GND
③ PTT
④ MIC
⑤ MIC GND
⑥ + 5V
⑦ UP
⑧ DOWN

| Pin 3 | PTT | Open Circuit Voltage: 5 V, Closed Circuit Current: 1 mA |
|---|---|---|

## GPS Jack

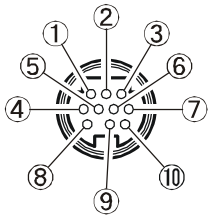
**(As Viewed From Rear Panel)**




① Connected with ④, ⑥, ⑦, and ⑧.
② GPS Data Input (+)
③ N/C
④ Connected with ①, ⑥, ⑦, and ⑧.
⑤ GPS Data Input (–)
⑥ Connected with ①, ④, ⑦, and ⑧.
⑦ Connected with ①, ④, ⑥, and ⑧.
⑧ Connected with ①, ④, ⑥, and ⑦.
⑨ NC

## ACC Jack

**(As Viewed From Rear Panel)**

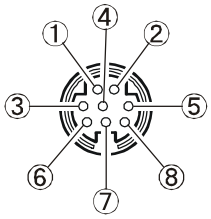



① +13.8 V OUT
② TX GND
③ GND
④ BAND DATA A
⑤ BAND DATA B
⑥ BAND DATA C
⑦ BAND DATA D
⑧ TX-INH
⑨ EXT ALC Input
⑩ TX REQ

| Pin 1 | +13.8 V | Max. 1 A<br>This terminal is connected in parallel with the pin 1 of TUNE Jack. |
|---|---|---|
| Pin 2 | TX GND | Open Collector<br>(Max. 60 V, 1A)<br>This terminal is connected in parallel with the pin 2 of TUNE Jack. |

## TUNE Jack

**(As Viewed From Rear Panel)**

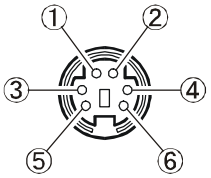



① +13.8 V OUT
② TX GND
③ GND
④ RX D
⑤ TX D
⑥ TUNER SENSE
⑦ RESET
⑧ TX-INH

| Pin 1 | +13.8 V | Max. 1 A<br>This terminal is connected in parallel with the pin 1 of ACC Jack. |
|---|---|---|
| Pin 2 | TX GND | Open Collector<br>(Max. 60 V, 1A)<br>This terminal is connected in parallel with the pin 2 of ACC Jack. |

## DATA Jack

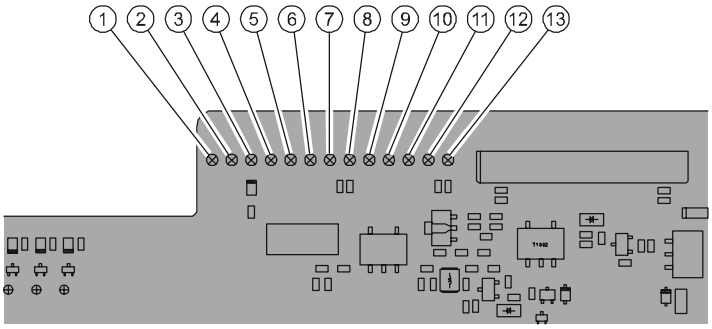
**(As Viewed From Rear Panel)**




① DATA IN
② GND
③ DATA PTT
④ DCD
⑤ DATA OUT
⑥ SQL OUT

| Pin 1 | DATA IN | 60 mVp-p @1 kΩ. |
|---|---|---|
| Pin 5 | DATA OUT | 500 mVp-p @1 kΩ |
| Pin 6 | SQL OUT | SQL OPEN: 5 V<br>SQL CLOSE: 0 V |

## Accessory Port (Located on the MAIN Unit)




① ENCR_TXIN
② ENCR_RXIN
③ INDICATOR
④ CODE (8)
⑤ CODE (4)
⑥ CODE (2)
⑦ CODE (1)
⑧ ENCR_RXOUT
⑨ CLEAR/SCRAMBLE
⑩ PTT
⑪ VCC
⑫ GND
⑬ ENCR_TXOUT